5x7mm Precision TCXO Model TV504DTR

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Description:

The Connor-Winfied TV504DTR is a 5x7mm voltage controlled surface mount temperature compensated crystal oscillator (VCTCXO). Through the use of analog temperature compensation, the TV504DTR is capable of holding ±0.25ppm temperature stability over the -10 to 70C temperature range.

Features:

- 3.3 Vdc Operation
- LVCMOS Output
- Frequency Stability: ± 0.25 ppm
- Temperature Range: -10 to 70°C
- Low Jitter <1ps RMS
- 5x7mm Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Pb Free

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	85	°C	
Supply Voltage (Vcc)	-0.5	-	6.0	Vdc	
Input Voltage	-0.5	-	Vcc+0.5	Vdc	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Nominal Frequency (Fo)		10.0		MHz	
Frequency Calibration @ 25 °C	-1.0	-	1.0	ppm	1
Frequency Stability vs. Temperature	-0.25	-	0.25	ppm	2
Holdover Stability (Over 24 Hours)	-0.32	-	0.32	ppm	3
Frequency vs. Load Stability	-0.05	-	0.05	ppm	±5%
Frequency vs. Voltage Stability	-0.05	-	0.05	ppm	±5%
Static Temperature Hysteresis	-	-	0.4	ppm	Absolute, 4
Total Frequency Tolerance:	-4.6	-	4.6	ppm	5
Operating Temperature Range:	-10	-	70	°C	
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	±5%
Supply Current (Icc)	-	-	6	mA	
Period Jitter	-	3	5	ps rms	
Integrated Phase Jitter	-	0.5	1.0	ps rms	6
Typical Phase Noise Fo = 10.0 MHz					
SSB Phase Noise at 10Hz offset	-	-99	-	dBc/Hz	
SSB Phase Noise at 100Hz offset	-	-122	-	dBc/Hz	
SSB Phase Noise at 1KHz offset	-	-145	-	dBc/Hz	
SSB Phase Noise at 10KHz offset	-	-152	-	dBc/Hz	
SSB Phase Noise at 100KHz offset	-	-153	-	dBc/Hz	
Start-up Time	-	-	10	ms	

Control Voltage Input Characteristics

ParameterMinimum	Minimum	Nominal	Maximum	Units	Notes
Control Voltage	0.3	1.65	3.0	V	
Frequency Pullability	±3	±4	±5	ppm	
Pull Slope (Vc=1.65V)	-	3.0	-	ppm/V	
Control Voltage Slope		Positive Slope			
Monotonic Linearity	-	-	5	%	
Input Impedance	100K	-	-	Ohm	
Modulation Bandwidth (3dB)	10	-	-	KHz	

LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	7
Voltage (High) (Voh)	90%Vcc	-	-	Vdc	
(Low) (Vol)	-	-	10%Vcc	Vdc	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	-	8	ns	

Notes:

1. *Initial calibration @ 25°C. Specifications at time of shipment after 48 hours of operation.*
2. *Frequency stability vs. change in temperature. [±(Fmax - Fmin)/(2*Fo)].*
3. *Inclusive of frequency stability, supply voltage change (±1%), load change, aging, for 24 hours.*
4. *Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C.*
5. *Inclusive of calibration @ 25C, frequency vs. change in temperature, change in supply voltage (±5%), load change (±5%), reflow soldering process and 20 years aging, referenced to Fo*
6. *BW = 12 KHz to Fo/2 MHz.*
7. *For best performance it is recommended that the circuit connected to this output should have an equivalent input capacitance of 15pF.*

RoHS COMPLIANT

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Package Characteristics

Package	Hermetically sealed crystal mounted on a ceramic package

Environmental Characteristics

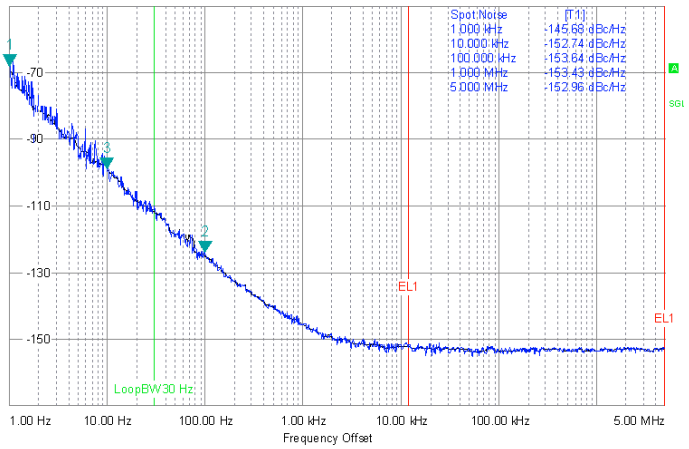
Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process;	RoHS compliant lead free. See soldering profile on page 2.

Ordering Information

TV504DTR-010.0M

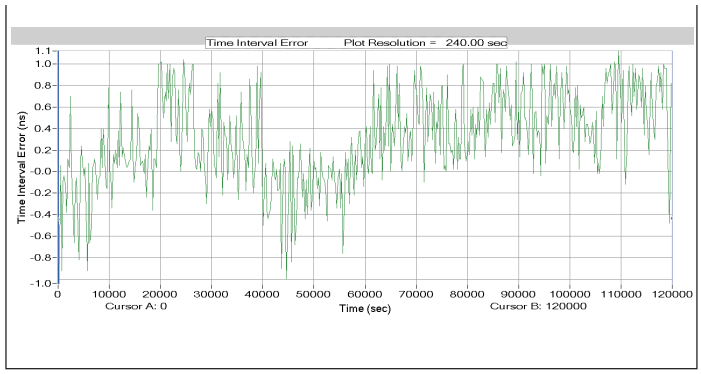
Phase Noise Information

Typical Phase Noise for TV504DTR-010.0M



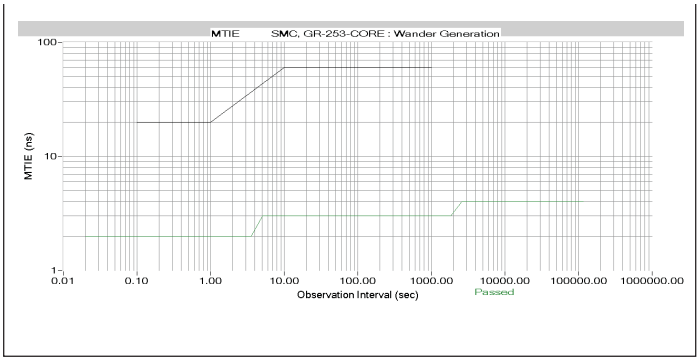
TIE

TV504DTR-010.0M: WANDER GENERATION IN A STRATUM 3 PLL AT 0.098 Hz BANDWIDTH



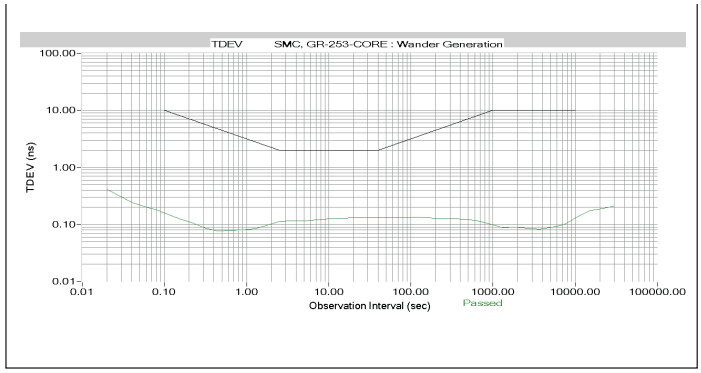
MTIE

TV504DTR-010.0M: MTIE per GR-253-CORE



TDEV

TV504DTR-010.0M: TDEV per GR-253-CORE



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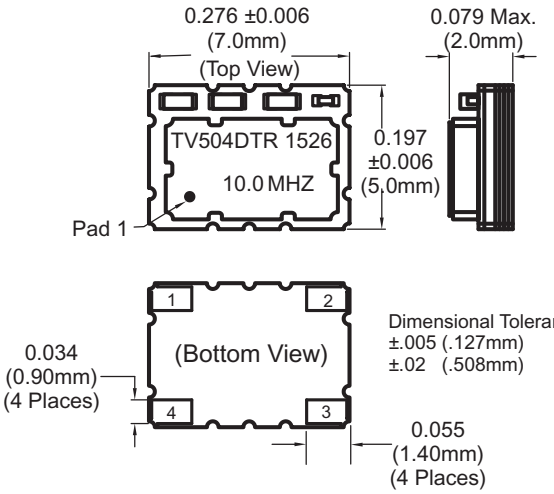
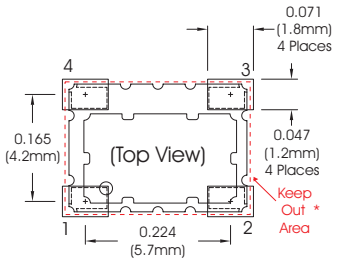
Package Layout



Suggested Pad Layout

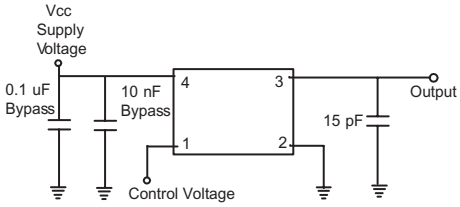


** Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.*

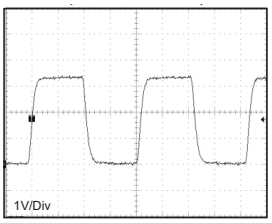
Pad Connections

1:	Control Voltage
2:	Ground
3:	Output (Fo)
4:	Supply Voltage (Vcc)

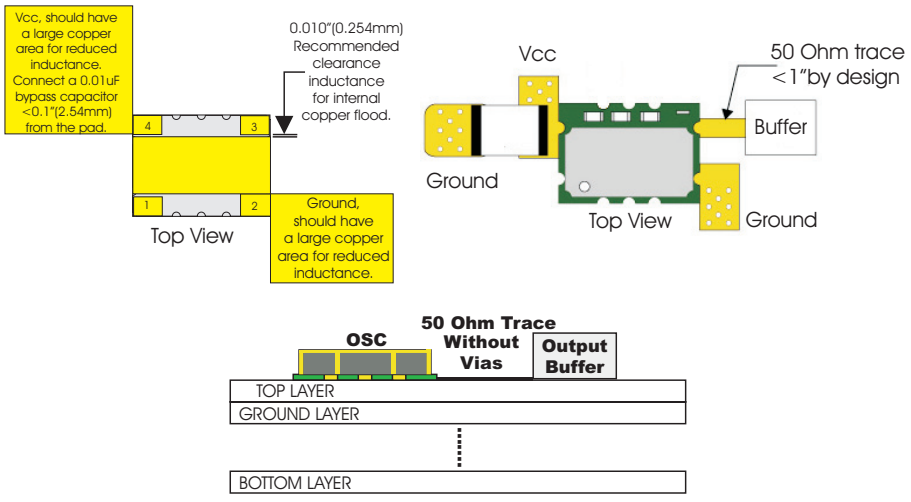
Test Circuit



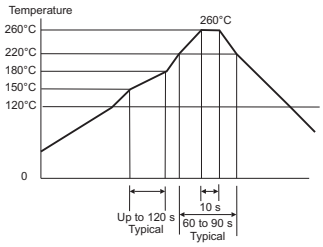
Output Waveform



Design Recommendations



Solder Profile



Meets IPC/JEDEC J-STD-020C

Attention: To achieve optimal frequency stability, and in some cases to meet the specification stated on this data sheet, it is required that the circuit connected to this TCXO output must have the equivalent input capacitance that is specified by the nominal load capacitance. Deviations from the nominal load capacitance will have a graduated effect on the stability of approximately 20 ppb per pF load difference.

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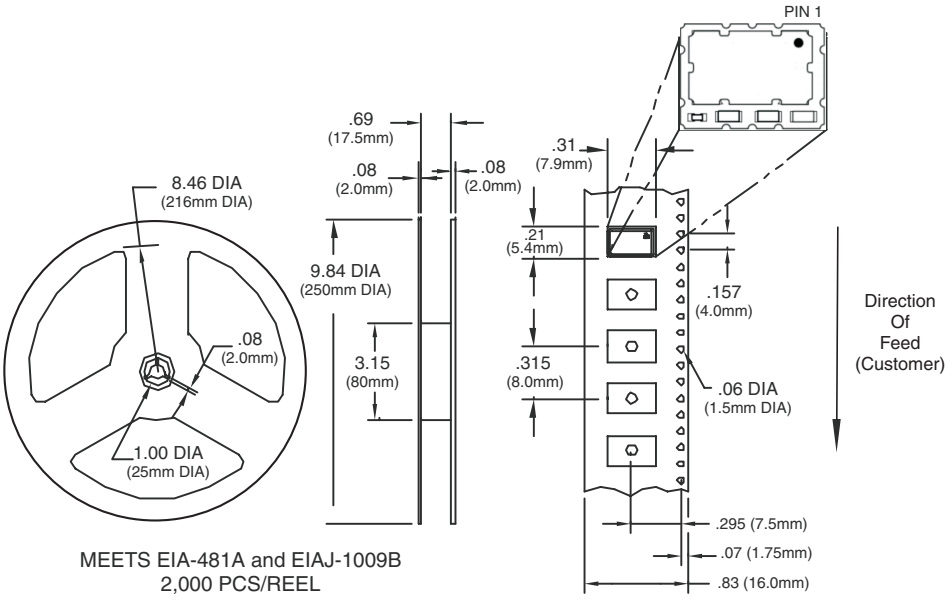
Applications:

- IEEE 1588 Applications
- Synchronous Ethernet slave clocks, ITU-T G.8262 EEC options 1 & 2
- Compliant to Stratum 3, GR-1244-CORE, GR-253-CORE & ITU-T-G.812 Type IV
- Wireless Communications
- Small Cells
- Test and Measurement

Tape and Reel Dimensions



MEETS EIA-481A and EIAJ-1009B
2,000 PCS/REEL

Revision History

Revision	Date	Note
00	06/23/15	Data sheet released